WHAT IS CLAIMED IS:

1. A semiconductor package comprising:

a plurality of horizontal metal leads, each lead having a first side, and an opposite second side having at least one horizontal first surface and at least one horizontal second surface recessed from the first surface;

a chip mounting substrate having a first side and an opposite second side, said second side having a horizontal central surface and a horizontal peripheral surface fully around and recessed from the central surface;

a semiconductor chip having an active surface facing the first side of the leads and the first side of the chip mounting substrate, and input-output pads at a peripheral portion of the active surface, wherein each of the peripheral input-output pads faces and is electrically connected to the first side of a respective one of the leads; and

a package body formed of a hardened encapsulating material, wherein the encapsulating material covers the semiconductor chip, the recessed peripheral surface of the second side of the chip mounting substrate, and the at least one recessed second surface of the second side of the leads, while the central surface of the second side of the chip mounting substrate and the at least one first surface of the second side of the leads are exposed at a horizontal first exterior surface of the package body.

2. The semiconductor package of claim 1, wherein the second side of each lead includes a plurality of the horizontal first surfaces and horizontal second surfaces, and the first surfaces of the leads collectively form rows and columns at the first exterior surface of the package body.

3. The semiconductor package of claim 1, wherein a surface of the semiconductor chip is exposed at an exterior surface of the package body.

4. The semiconductor package of claim 1, wherein the active surface of the semiconductor chip includes at least one central input-output pad inward of the peripheral input-output pads, and the at least one central input-output pad faces and is electrically connected to the first side of the chip mounting substrate.

5. The semiconductor package of claim 4, where the peripheral input-output pads and the at least one central input-output pad of the chip are each electrically connected to the first side of the lead or the first side of the chip mounting substrate, respectively, by a reflowed metal ball.

6. The semiconductor package of claim 5, further comprising a discrete insulative layer on the first side of each of the leads and the first side of the chip mounting substrate, wherein the insulative layer is covered by the encapsulating material and the respective reflowed metal ball extends through an opening in the respective insulative layer.

7. The semiconductor package of claim 4, where the peripheral input-output pads and the at least one central input-output pad of the chip are each electrically connected to the first side of the lead or the first side of the chip mounting substrate, respectively, by an anisotropic conductive film.

8. The semiconductor package of claim 1, where the peripheral input-output pads of the chip are each electrically connected to the first side of the respective lead by a reflowed metal ball.

9. The semiconductor package of claim 8, further comprising a discrete insulative layer on the first side of each of the leads, wherein the insulative layer is covered by the encapsulating material and the respective reflowed metal ball extends through an opening in the respective insulative layer.

10. The semiconductor package of claim 1, where the peripheral input-output pads of the chip are each electrically connected to the first side of the respective lead by an anisotropic conductive film.

11. The semiconductor package of claim 1, further comprising a conductive ball fused to each exposed second surface of the second side of the leads.

12. The semiconductor package of claim 2, further comprising a conductive ball fused to each exposed first surface of the second side of the leads.

13. The semiconductor package of claim 11, wherein a conductive paste or a plurality of conductive balls are on the central surface of the second side of the chip mounting substrate.

14. A semiconductor package comprising:

a plurality of horizontal metal leads, each lead having a first side, and an opposite second side having at least one horizontal first surface and at least one horizontal second surface recessed from the first surface;

a chip mounting substrate having a first side and an opposite second

side, said second side having a horizontal central surface and a horizontal peripheral surface fully around and recessed from the central surface;

a semiconductor chip in a flip chip electrical connection with the first side of the leads and the first side of the chip mounting substrate; and

a package body formed of a hardened encapsulating material, wherein the encapsulating material covers the semiconductor chip, the recessed peripheral surface of the second side of the chip mounting substrate, and the recessed second surface of the second side of the leads, while the central surface of the second side of the chip mounting substrate and the at least one first surface of the second side of the leads are exposed at a horizontal first exterior surface of the package body.

15. The semiconductor package of claim 14, further comprising a discrete insulative layer on the first side of the leads and the first side of the chip mounting substrate, wherein the insulative layer is covered by the encapsulating material, and the chip is electrically connected to the first side of the respective lead and the first side of the chip mounting substrate through an opening in the respective insulating layer.

16. A semiconductor package comprising:

a plurality of horizontal metal leads, each lead having a first side, and an opposite second side having at least one horizontal first surface and at least one horizontal second surface recessed from the first surface;

a chip mounting substrate having a first side and an opposite second side, said second side having a horizontal central surface and a horizontal peripheral surface fully around and recessed from the central surface;

a plurality of insulative layers, wherein a respective one of the insulative layers is on the first side of the leads and the first side of the chip

mounting substrate;

a semiconductor chip in a flip chip electrical connection with the first side of the leads and the first side of the chip mounting substrate through the respective insulative layer; and

a package body formed of a hardened encapsulating material, wherein the encapsulating material covers the semiconductor chip and the insulative layers, the recessed peripheral surface of the second side of the chip mounting substrate, and the recessed second surface of the second side of the leads, while said central surface of the second side of the chip mounting substrate and the at least one first surface of the second side of the leads are exposed at a horizontal first exterior surface of the package body.